DETAILED ACTION

Status of Claims

Claims 1-43 have been presented for examination in this application.

Claims 44-53 have been added.

Claims 1-39 have been canceled.

Claims 40-53 remain pending.

Claims 40-53 are allowed.

Applicant's remarks and amendments filed 3/16/2010 have been considered with the results that follow.

All rejections and objections not explicitly repeated below are withdrawn.

Information Disclosure Statement

The Information Disclosure Statements received 12/18/2009 and 12/21/2009 have been considered. However, in the IDS submitted on 12/21/2009, foreign patent document EP 0910021 is not considered, since it does not have an English translation. See attached PTO-1449(s).

Examiner's Amendment

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1 .312.To ensure consideration of such an amendment, it must be submitted no later than the payment of the issue fee.

Authorization for the examiner's amendments to the claims was given in a telephone interview with Karen M. Henckel #58371 on 5/15/2010. The application has been further amended as follows:

As in claim 40,

" A method for executing read and write commands in a memory system having a bidirectional memory bus coupling a controller to a first, second, and third memory hub, the second memory hub being downstream from the first memory hub, and the third memory hub being downstream from the second memory hub, the method comprising:

the controller issuing a read command to access a first memory location in a first memory device coupled to the second memory hub;

after the controller issues the read command and before receiving ~~the~~ read data corresponding to the issued read command, the controller issuing a write command to write data to a second memory location in a second memory device coupled to the third memory hub, the controller further providing write data corresponding to the issued write command to the bi-directional memory bus;

retrieving the read data ~~corresponding to the issued read command~~ from the first memory location and providing the read data to the bi-directional memory bus;

the controller providing a bypass enable signal to the first memory hub;

in response to receiving the bypass enable signal, the first memory hub storing the write data to allow the read data on the bidirectional memory bus to be coupled to the controller; and

the first memory hub providing the write data to the bidirectional memory bus.”.

As in claim 44,

“ A method for writing data to a memory location in a memory system, the memory system including a controller coupled to a first, second, and third memory hub by a bidirectional memory bus, the second memory hub being located downstream from the first memory hub, the third memory hub being located downstream from the second memory hub, the method comprising:

the controller issuing a read command to a first memory location of a first memory device coupled to the second memory hub;

after the controller issuing the read command and before receiving corresponding read data, the controller issuing a write command to a second memory location of a second memory device coupled to the third memory hub and providing write data corresponding to the issued write command to the bidirectional memory bus;

coupling the read data corresponding to the previously issued read command to the bidirectional memory bus;

the controller ~~or a memory hub~~ providing a bypass enable signal to the first memory hub;

in response to the bypass enable signal, the first memory hub coupling the write data to a register in the memory system for temporary storage of the

write data to allow the read data corresponding to the previously issued read command to propagate on the bidirectional data bus;

recoupling the write data stored in the register to the bidirectional memory bus; and

writing the write data to the memory location. ".

As in claim 48,

" A method for executing memory commands in a memory system having a bidirectional memory bus on which both read and write data can be coupled, the memory system including a controller coupled to a first, second, and third memory hub, the second memory hub being downstream from the first memory hub, the third memory hub being downstream from the second memory hub, the method comprising:

the controller issuing a read command to a first memory location in a first memory device coupled to the second memory hub;

the controller issuing a write command to a second memory location in a second memory device coupled to the third memory hub and providing write data corresponding to the write command to the bidirectional memory bus of the memory system after issuing the read command;

accessing read data from the first memory location, the read data corresponding to the previously issued read command;

coupling the read data corresponding to the previously issued read command to the bidirectional memory bus;

the controller ~~or a memory hub~~ providing a bypass enable signal to the first memory hub;

in response to the bypass enable signal, decoupling the write data in the first memory hub from the bidirectional memory bus preventing a collision between the read data and the write data;

propagating the read data on the bidirectional memory bus through the first memory hub; and

recoupling the write data to the bidirectional memory bus. " .

As in claim 52,

" A memory system comprising:

a bidirectional memory bus;

a controller coupled to a first, second, and third memory hub, the second memory hub being downstream from the first memory hub, and the third memory hub being downstream from the second memory hub; the controller coupled to the bidirectional memory bus, wherein the controller is configured to issue a read command to access a first memory location in a first memory device coupled to the second memory hub;

after the controller issues the read command and before receiving read data corresponding to the issued read command, the controller issuing a write command to write data to a second memory location in a second memory device coupled to the third memory hub, the controller further providing write data corresponding to the issued write command to the bi-directional memory bus,~~and~~

~~write commands and to issue write data to a bidirectional memory bus,~~ the controller further configured to issue a bypass enable signal; and

the [[a]] first memory hub[coupled to the controller by the bidirectional memory bus, the first memory hub] including a bypass circuit configured to receive the write data from the bidirectional memory bus and to store the write data in response to receiving the bypass enable signal from the controller, ~~; and~~

~~a second memory hub coupled to the first memory hub and the controller by the bidirectional memory bus, the second memory hub coupled to at least one memory device and located down stream from the first memory hub, the second memory hub configured to provide read data to the bidirectional memory bus~~

wherein the bypass circuit is configured to store the write data in the first memory hub in response to receiving the bypass enable signal to allow the read data to propagate on the bidirectional memory bus passed the write data in the first memory hub ~~through the first memory hub~~ and to prevent a data collision between the read data and the write data on the bidirectional memory bus.

Allowable Subject Matter

The art of record neither teaches nor fairly suggests the method of independent claim 40 including the following combination of limitations defining the main invention/embodiment:

" .. method for executing read and write commands in a memory system having a bidirectional memory bus coupling a controller to a first, second, and third memory hub, the second memory hub being downstream from the first

memory hub, and the third memory hub being downstream from the second memory hub ..

.. after the controller issues the read command and before receiving the read data. The controller issuing a write command to write data to a second memory location in a second memory device coupled to the third memory hub, the controller further providing write data corresponding to the issued write command to the bi-directional memory bus

… the controller providing a bypass enable signal to the first memory hub;

.. in response to receiving the bypass enable signal, the first memory hub storing the write data to allow the read data on the bidirectional memory bus to be coupled to the controller; and the first memory hub providing the write data to the bidirectional memory bus “

Claims 44 and 48 contains allowable subject matter since they have similar limitations of claim 40 as discussed above.

Claim 52 directs to a memory system and contains allowable subject mater since it has similar limitations of claim 40 as discussed above.

The remaining dependent claims, not specifically mentioned, are allowed for the same rationale as the independent claim(s) being based from.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00

PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

/Tuan V. Thai/

Primary Examiner, Art Unit 2185